

Status of Claims

Claims 1, 4, 5 and 7 through 12 are pending in the application. Claims 1, 4, 5 and 7 through 12 have been rejected. Claim 1, 4, 5 and 7 have been amended.

The Telephone Interview

Initially, Applicant wishes to thank the Examiner, Chandra Chaudhari, for granting and attending the telephone interview, with Applicant's Representative, Vladimir Sherman, Reg. No. 43,116 on Tuesday November 26, 2002. In the interview, claims 1, 4, 5 and 7 through 12 were discussed, as where the Examiner's cited prior art references; (1) Hayabuchi – U.S. Pat. No. 5,324,675, and (2) Chang – U.S. Pat. No. 5,836,772.

During the Interview, Applicant pointed out to the Examiner portions of the specification teaching various claimed limitations which the Examiner was unable to find during his first review of the present application. Applicant and the Examiner agreed to replace the term "generally" with the term "substantially" in claims 1, 4, 5 and 7 in order to overcome the Examiner's 112 rejections of those claims. Furthermore, Applicant has agreed to amend a range value in claim 7, so as to harmonize claim 7 with dependent claim 10 and the specification.

Regarding Examiner's cited references, Applicant has agreed to amend claims 1, 4, 5 and 7 to clearly recite that oxygen is introduced into a memory cell's nitride layer in order to enhance charge retention of the nitride layer. Given that all of the Examiner's cited references teach of semiconductor elements which do not store or retain charge in a nitride layer, but rather use the nitride layer as part of an insulator, it is believed that the agreed upon amendments should sufficiently distinguish claims 1, 4, 5, and 7 from the cited references.

Claim Rejections

35 U.S.C. § 112 Rejections

In the Office Action, the Examiner rejected claims 1, 4, 5 and 7 through 12 under 35 U.S.C. § 112, first paragraph, for allegedly "containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art the inventor(s), at the time the application was filed, had possession of the claimed invention." (Office Action, Page 2, Last Paragraph)

In the Office Action, the Examiner rejected claims 1, 4, 5 and 7 through 12 under 35 U.S.C. § 112, second paragraph, for allegedly “being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.” (Office Action, Page 3, First Paragraph)

More specifically, the Examiner alleges that the limitation “[introducing oxygen] into generally all of said nitride layer,” as recited in claims 1, 4, 5 and 7 is not supported by the specification, in addition to being unclear in meaning.

In response to this rejection, Applicant wishes to bring the Examiner’s attention to a portion of the specification between page 7, line 24 and page 8, line 24. Within the body of the text, it is taught that “during oxidation of a top layer, some of the oxygen is introduced into the non-consumed nitride layer... [and] the concentration can range from a low 10% to a high 80%”. Also, “in order to produce a retention layer, which provides effective charge retention, it is recommended to introduce a high percentage of oxygen into the nitride. [However, there may be instances when the] oxygen introduced into the oxygen rich nitride layer [may] reach the silicone oxide...”

It is Applicant’s position that from the above-cited portion of the specification, it would be quite clear to one of ordinary skill in the art how and why to introduce “oxygen into generally all of said nitride layer.” During a telephone interview with the Examiner, the Examiner stated that he found the term “generally all” to be objectionable and/or unclear. Therefore, for purposes of expediting prosecution, it has been agreed to replace the term “generally” with the term “substantially.” Applicant has amended claims 1, 4, 5 and 7 to recite: “introducing oxygen into substantially all of said nitride layer....” In view of the above clarification and amendment, Applicant respectfully requests the Examiner to withdraw the above-stated 112 rejection of claims 1, 4, 5 and 7 and any claims which depend there-from.

The Examiner also alleges that the limitation “wherein said nitride layer is 100 angstroms or less thick”, as recited in claim 7 is not supported by the specification. In response to this rejection, Applicant wishes to bring the Examiner’s attention to Page 7, Lines 19 to 25 of the specification, where it is written that “A nitride layer is then deposited over bottom oxide layer to a thickness of between 20 Angstroms and 150 Angstroms where a preferred thickness is as thin as possible, such as 10 Angstroms - 50 Angstroms.” Certainly the Examiner can not argue against the fact that a nitride thickness of “10 Angstroms - 50

Angstroms”, as stated in the specification, supports the recited limitation of “100 angstroms or less.”

However, for purposes of expediting prosecution, Applicant has amended claim 7 more closely recites the teachings of the specification: “wherein said nitride layer is 150 angstroms or less thick.” In view of the above clarification and amendment, Applicant respectfully requests the Examiner with withdraw the above-stated 112 rejection of claims 7.

The Examiner also rejected claim 10 for being unclear because it states “a nitride layer of approximately 20-150 angstroms thick, whereas claim 7 states the nitride layer is 100 angstroms or less.” Claim 7 has been amended to recite that the nitride layer may be “150 angstroms or less,” which amendment is supported by the specification, as explained above. Therefore the Examiner’s 112 rejection of claim 10 is rendered moot. Applicant respectfully requests that the Examiner withdraw the above-stated 112 rejection of Claim 10.

Applicant respectfully asserts that all the claims are proper under 35 USC § 112 and request that all 112 rejections be withdrawn.

35 U.S.C. § 102 Rejections

Claims 1, 4, 5 and 7 stand rejected under 35 U.S.C. § 102 (b) as being anticipated by Hayabuchi - US 5,324,675 or, alternatively, under 35 U.S.C. § 102 (e) as being anticipated by Chang - US 5,836,772. Applicant respectfully traverses these rejections in view of the remarks that follow.

Claims 1, 4, 5 and 7 each recite the limitation of “Introducing oxygen into generally all of said nitride layer within said memory cell, so as to enhance charge retention within said nitride layer.”

Hayabuchi discloses:

“A method of producing a semiconductor device of the type which includes a semiconductor substrate; a gate insulating layer of a triplex structure formed on the semiconductor substrate and composed of a first oxide layer, an oxidation-resistant layer and a second oxide layer, and a gate electrode formed on the gate insulating layer, includes the steps of: forming the first oxide layer, the oxidation-resistant layer, and the second oxide layer successively on the semiconductor substrate; adjusting the thickness of the oxidation-resistant

layer during or after the formation thereof in such a way that the entire oxidation-resistant layer can be oxidized in a post-process in which the oxidation-resistant layer is oxidized except for that region which corresponds to the gate electrode; and oxidizing the oxidation-resistant layer except for the region corresponding to the gate electrode and forming an oxide layer around the gate electrode, whereby the oxidation-resistant layer is entirely oxidized except for the region corresponding to the gate electrode. The resulting silicon oxide layer can be used as an address gate or as the gate insulating layer of an MOS transistor gate for a peripheral circuit.” (Abstract)

As is evident from the Hayabuchi Abstract, the oxidation of oxidation-resistant layer, which may be silicon nitride, is done so as to form an insulating layer and not a charge retention layer, as is claimed in claims 1, 4, 5 and 7. Hayabuchi is very clear and repeats numerous times that “the oxidation-resistant layer is entirely oxidized except for the region corresponding to the gate electrode.” For example, “Here, the thickness of the silicon nitride layer 4 is determined such that it can be entirely oxidized in a post-process described below, in which the silicon nitride layer 4 is oxidized except for the region thereof corresponding to the gate electrode described below” (col. 3, lines 61 – 65). Hayabuchi teaches oxidized nitride as a insulator not as active charge retention layer.

Hayabuchi, therefore, clearly teaches away from “causing oxygen to be introduced into substantially all of said nitride layer within said memory cell so as to enhance charge retention within said nitride layer”, which is a limitation present in each of the independent claims (1, 4, 5 and 7).

In order to support a rejection under 35 U.S.C. § 102 (b), the Examiner needs to provide a single reference which teaches all of the limitations of the rejected claim or claims. The Hayabuchi reference, however, does not seem to teach the limitation of “causing oxygen to be introduced into substantially all of said nitride layer within said memory cell so as to enhance charge retention within said nitride layer”. To the contrary, the Hayabuchi reference teaches not to oxidize a silicon nitride layer in a region corresponding to the gate electrode. Therefore, it would appear the Examiner has not met the requirements for supporting the 35

U.S.C. § 102 (b) rejection for claims 1, 4, 5 and 7, and Applicant respectfully requests reconsideration of these claims and all the claims that depend thereon.

Chang et al. discloses:

"A process is provided for fabricating a nonvolatile memory cell. According to the process, source and drain regions are formed on a first conductivity-type semiconductor substrate; and insulating layer is formed on the source and drain regions; a floating gate is formed on the insulating layer; a dielectric composite is formed on the floating gate; and a control gate is formed on the dielectric composite. The dielectric composite includes a bottom layer of silicon dioxide formed on the floating gate; a layer of silicon nitride formed on the bottom silicon dioxide layer; and a top layer of silicon dioxide formed on the nitride layer such that the silicon nitride layer of the composite is thinner than the top or the bottom silicon dioxide layer." (Abstract)

The only mention made of introducing oxygen into any of the silicon nitride layer is found in statements such as: "Pinholes in the silicon nitride layer are preferably plugged with oxygen, most preferably by thermal treatment prior to formation of the top layer of silicon dioxide on the nitride layer" (Col. 2, lines 62 – 65). The reason being that Chang teaches using a oxide-nitride-oxide sandwich as an insulator and not as a charge retention structure.

Chang et al., therefore, does not teach or suggest "causing oxygen to be introduced into substantially all of said nitride layer within said memory cell, so as to enhance charge retention within said nitride layer," a limitation found in each of claims 1, 4, 5 and 7. Since Chang et al. only teaches to fill the pinholes during a process between formation of the nitride layer and that of the top silicon dioxide layer, and solely for the purpose of forming a better insulation layer, Chang et al. cannot anticipate claims 1, 4, 5 and 7 under 35 U.S.C. § 102 (e).

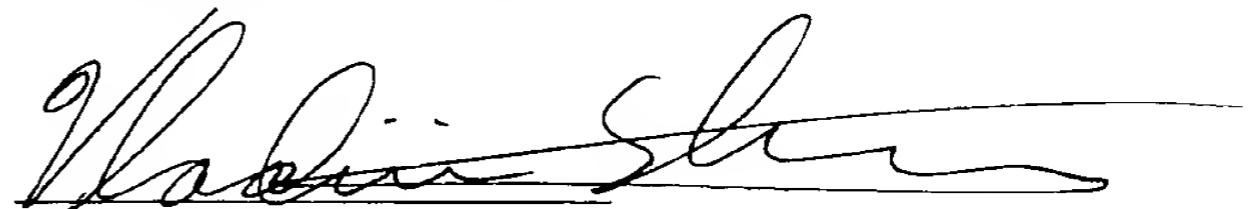
In view of the foregoing amendments and remarks, the independent claims 1, 4, 5 and 7 are believed to be allowable. Their favorable reconsideration and allowance is respectfully requested. Furthermore, all claims depending from claims 1, 4, 5 and 7 should now also be allowable by virtue of their dependency from allowable base claims. Their favorable reconsideration and allowance is also respectfully requested.

Should the Examiner have any question or comment as to the form, content or entry of this Amendment, the Examiner is requested to contact the undersigned at the telephone

number below. Similarly, if there are any further issues yet to be resolved to advance the prosecution of this application to issue, the Examiner is requested to telephone the undersigned counsel.

Please charge any fees associated with this paper to deposit Account No. 05-0649.

Respectfully submitted,



Vladimir Sherman
Attorney for Applicant(s)
Registration No. 43,116

Dated: December 2, 2002

Eitan, Pearl, Latzer & Cohen-Zedek
One Crystal Park, Suite 210, 2011 Crystal Drive
Arlington, VA, USA 22202-3709
Telephone: (703) 486-0600
Fax: (703) 486-0800

VERSION WITH MARKINGS TO SHOW CHANGES MADE

In the Claims:

Kindly amend claims 1, 4, 5 and 7 as follows:

1. A method of fabricating an oxide-nitride-oxide (ONO) layer in a memory cell, said method comprising:

forming a bottom oxide layer on a substrate;
depositing a nitride layer; and
oxidizing a top oxide layer, thereby causing oxygen to be introduced into [generally] substantially all of said nitride layer within said memory cell, so as to enhance charge retention within said nitride layer.

4. A method for improving the charge retention in a nitride layer of a memory cell, said method comprising:

depositing a nitride layer; and
introducing oxygen into [generally] substantially all of said nitride layer within said memory cell, so as to enhance charge retention within said nitride layer.

5. A method for improving the charge retention in a nitride layer of a memory cell, said method comprising:

depositing a nitride layer;
controlling the thickness of said deposited nitride layer; and
introducing oxygen into [generally] substantially all of said nitride layer within said memory cell, so as to enhance charge retention within said nitride layer.

7. A method of manufacturing a programmable, read only memory device, the method comprising:

forming a first oxide layer on a substrate,
forming a nitride layer on top of said oxide layer, wherein said nitride layer is [100] 150 angstroms or less thick;

introducing oxygen into [generally] substantially all of said nitride layer within a memory cell during formation of a second oxide layer on top of said nitride layer, so as to enhance charge retention within said nitride layer;

patterning said oxide-nitride-oxide (ONO) layers into desired patterns; and forming a gate layer over said patterned ONO layer.